# Data Recovery

Field of the Invention

This invention relates to a data recovery apparatus and method, and more particularly, to error detection and/or correction in data recovery apparatus, and a method of recovering, in digital format, analogue data recorded on a medium, such as a tape.

Background to the Invention

It is known to use an analogue chip to recover, in digital format, analogue data which is recorded on a medium, such as a tape. Referring to Figure 1 of the drawings, which illustrates a simplified version of such analogue chip, such a data recovery circuit generally comprises a variable gain amplifier (VGA) 100, which receives analogue data 102 from a tape (not shown), a filter 104 to smooth the analogue wave form, and analogue-to-digital converter (ADC) 106 for converting the smoothed analogue waveform 108 into a 6-bit digital signal, a digital signal processing module 110, a Viterbi detector 112 to produce 6-bit RRL decoder 114 which produces 4-bit output data.

The output from the RLL decoder 114 is then input to an error correction circuit (not shown). In general, the number of errors which known error correction circuits can detect and/or correct is dependent on the number of parity symbols which are added to the data. An error in a code word has two unknown quantities, namely its location and the amount by which a symbol is incorrect. If, for example, four parity symbols are added to each code word, a conventional error detection/correction circuit can deal with four unknown quantities, i.e. two errors. If, however, the location of an error is known, there is only one unknown quantity, so the circuit can handle up to four errors in a code word if their locations are known. The term used to describe an error whose location is known is an "erasure", and, in general, conventional error correction circuits can correct twice as many erasures as errors.

When analogue data is read from a tape (not shown), it is common for errors to occur, which result in bad data being read. For example, the tape may flap away from the

tape head ("drop-out") or the temperature of a magneto resistive head may suddenly change, causing a thermal asperity. A change in the head temperature causes a change in the head resistance resulting in a DC shift in the analogue signal. The temperature of the head can change suddenly when a piece of dust or debris on the tape hits the head. The dust or debris either heats the head due to friction, or cools the head by conduction. The tape channel is AC coupled to the head so, after a certain amount of time (dependent upon the magnitude of the DC shift), the signal comes back into range. However, in the meantime, the DC shift can cause the timing lock of the clock 116, which controls the sampling time of the analogue-to-digital converter 106, to be lost. To prevent or rectify this problem, the conventional circuit includes a thermal asperity detector 118, the output of which is fed to the digital signal processing module 110, which controls the timing recovery circuit 120.

During normal operation, the digital signal processing module 110 performs phase adjustments in a timing recovery circuit 120. However, in the event that a thermal asperity is detected, the digital signal processing module 110 allows the timing recovery circuit 120 to coast over known bad areas, i.e. in effect, it does not update the phase adjustments in the timing recovery circuit 120, thereby ensuring that erroneous data does not adjust the position of the sampling point.

In the conventional circuit, however, the output from the digital signal processing module 110 is still fed to the Viterbi detector 112 which outputs the most likely sequence of data to be input to the RLL decoder 114. Detector 112 does not known that the data it is processing is bad data and outputs a sequence of data to the RLL decoder 114 in the usual manner. Not every sequence of bits is a valid RLL encoded sequence, and the RLL decoder marks such invalid sequences as errors by setting an erasure flag to 1. The erasure flag is 0 if the sequence is a valid RLL encoded sequence.

In the prior art circuit, though, some of the data sequences output by the Viterbi detector 112 in response to bad data are valid RLL encoded sequences (even though they are incorrect) and, as such, are not recognised as errors so no erasure flag is set. Nevertheless, as stated above, it is highly desirable for the error correction circuit (not shown) to know the location of errors, as this doubles its error correction capability.

EP-A-0926671 describes a data recovery circuit similar to the one described above, in which a thermal asperity detector is provided. The output from the RLL decoder is still output from the circuit. In addition, this output is fed into an error generation circuit, together with the output from the thermal asperity detector, and the output from the error generation circuit (which comprises an error signal indicating data sequences which are incorrect due to thermal asperity having occurred) is also output from the circuit. Thus, the arrangement described in EP-A-0926671 is an ASIC (Application Specific Integrated Circuit) having two separate outputs, one for the data itself, and one for the error signal.

In order to communicate the outputs generated by the above-described ASIC, therefore, an additional pin/line is required. However, it is highly desirable to minimise the pin count and communications lines between ASICs because:

(a) an increase in the number of pins causes a corresponding increase in size of the ASIC package, which increases its consumption of circuit board space accordingly;

(b) each pin in an ASIC requires a pad on a silicon wafer in the package, with each pad taking up space, potentially wasting silicon and increasing the price of the ASIC; thus, the above-mentioned increase in number of pins on the ASIC is for this reason undesirable;

(c) the larger the number of electrical communication lines in a package, the higher its power consumption is, which is again undesirable.

US patent 5,373,513 describes a decoder for receiving and recovering encoded data. The decoder includes a peak polarity processor which senses the presence of the additive errors in the playback RLL data. The peak polarity processor classifies each additive error as either a drop-in or drop-out error and flags the affected code symbol location to the decoder as an erasure.

WO 99/18575 describes a decoder in which a thermal asperity detector is provided. When thermal asperity is detected, an event signal is fed back to activate a squelch circuit which removes large offsets caused by the thermal asperity while leaving minimal transient before the digital signal is fed to the Viterbi detector.

Summary of the Invention

In accordance with one aspect of the present invention, a decoding apparatus for the recovery of encoded data comprises an analogue-to-digital converter for receiving an analogue input signal and converting it into a digital signal, a detector for producing sequences of data representative of the analogue signal, and a decoder arranged to output data indicating that a sequence includes an error. The apparatus further comprises an event detector for detecting an event which substantially alters or destroys the analogue input signal. The detector has an input responsive to one or more event signals indicating the occurrence of such an event in response to which the detector responds to the one or more event signals by outputting one or more invalid data sequences. The decoder outputs a data stream representing the analogue input signal and including data corresponding to the or each sequence resulting from the altered or destroyed analogue input signal indicating that the sequence is incorrect.

Also in accordance with the present invention, a method of recovering encoded data comprises the steps of receiving an analogue input signal and converting it into a digital signal, producing sequences of data representative of the analogue signal, decoding the sequence of data, and outputting it together with data indicating whether or not a sequence includes an error. The input signal is monitored and an event which substantially alters or destroys the analogue input signal is detected. One or more event signals indicating the occurrence of such an event is produced. In response to the one or more event signals one or more invalid sequences of data are produced. A single communication path outputs a data stream representing the analogue input signal and including data corresponding to the or each sequence resulting from the altered or destroyed analogue input signal to indicate that the sequence is incorrect.

Thus the present invention provides an improved apparatus for and method of indicating the positions of errors in a data stream, being communicated between two ASICs for example, where the read channel expects there to be errors in the data stream, due for example, to mis-detection or thermal asperity events which severely distort the incoming signal. The error signal is delivered from the read channel detector using the same communication line (both physically and functionally) in the ASIC as is used to deliver the digital data itself. Thus, the functionality of the prior

art is achieved without an increase in the number of pines/lines required between different ASICs.

An object of the invention is achieved, in a specific embodiment, by intentionally transmitting a predetermined pattern which does not comply with RLL decoder rules, rather than the erroneous data stream. The predetermined violating pattern in the receiving ASICs decoder marks the position of specific types of errors in the data stream. Preferably, the event detector is coupled or connected to the detector for producing a sequence of data representative of the analogue signal or to the decoder.

In one preferred embodiment therefore, the detector is a Viterbi detector which receives the digital input signal and produces the most likely resultant sequence of data. The decoder is preferably an RLL decoder which decodes the sequence of data and produces n-bit code words which are output together with a flag which is set to 0 if the code word is thought to be correct, and 1 if the input sequence is recognised as being invalidly RLL encoded. Thus, as described above, in a preferred embodiment of the invention, the detector is arranged to output an input sequence which is known to be validly RLL encoded if the event detector detects an event which substantially alters or destroys the corresponding analogue input signal.

In other words, in the case where the event detector is connected to the (Viterbi) detector, the event detector forces the detector to output an invalid (RLL) encoded sequence of data, which results in the decoder outputting code words having the error flag set to 1 representative of the duration of the event. In the case where the event detector is connected directly to the decoder, however, it simply causes the decoder to output code words with the erasure flag set to 1 for the duration of the event.

The event detector is beneficially a thermal asperity detector, although it is envisaged that apparatus for detecting "drop-outs" and the like can be alternatively or additionally used. The thermal asperity (or other event) detector is preferably connected or coupled to the (Viterbi) detector or the (RLL) decoder by a shift or delay circuit.

In the case where the event detector is a thermal asperity detector, this preferably holds predetermined positive and negative thresholds and, if the analogue input signal exceeds the positive and/or goes below the negative threshold for more than a predetermined period of time, thermal asperity is indicated to have occurred. The event detector preferably outputs one or more signals indicating that an event is occurring until the event terminates; in this case, such an event signal would be output for the period of time during which the signal is outside the threshold value(s).

Brief Description of the Drawings

An embodiment of the invention will now be described by way of example only and with reference to the accompanying drawings, in which:

Figure 1, as described, is a simplified schematic block diagram of a decoding circuit according to the prior art; and

Figure 2 is a simplified schematic block diagram of a decoding circuit according to an exemplary embodiment of the present invention.

Detailed Description of the Invention

Figure 2 includes many of the same components as the circuit shown in Figure 1, and like components between Figures 1 and 2 are denoted by the same reference numerals.

In Fig. 2, however, the thermal asperity detector 118 is also connected to the Viterbi detector 112 via a shift register or delay circuit 122. The thermal asperity detector 118 holds positive and negative thresholds and operates in accordance with an algorithm which states that if the analogue waveform read from the tape exceeds the positive or drops below the negative threshold for more than a predetermined period of time, then thermal asperity has occurred. The thermal asperity detector 118 sends one or more event signals to the Viterbi detector 112 indicating that thermal asperity has occurred and continues to send such event signals until the thermal asperity ends, i.e. the input signal returns to a value within the threshold(s).

Viterbi detector 112 responds to receipt of the signal from the thermal asperity detector 118 to produce invalid RLL encoded data sequences for the duration of the bad data caused by thermal asperity, thereby causing the RLL decoder 114 to produce erasures for each sequence resulting from the bad data.

Thus, the error correction capability of the error detection and/or correction circuit (not shown) is greatly improved by marking known bad data as erasures.

Of course, the output of the shift register 122 could be connected directly to the RLL decoder 114, thereby causing the RLL decoder to set the erasure flags for each sequence of data resulting from the bad data. However, this is only really practical if the RLL decoder is on the same chip as the thermal asperity detector, which it often is. Otherwise, additional pins and connections would be necessary.

While a particular embodiment of the present invention has been shown and described in detail herein, it may be obvious to those skilled in the art that changes and modifications to the present invention in its various aspects, may be made without departing from the invention in its broader aspects, some of which changes and modifications being matters or routine engineering or design, and others being apparent after study. As such, the scope of the invention should not be limited by the particular embodiments and instructions described herein, but should be defined by the appended claims and equivalents thereof. Accordingly, the aim of the appended claims is to cover all such changes and modifications as fall within the true scope of the invention.